LM134/LM234/LM334 3-Terminal Adjustable Current Sources

Check for Samples: LM134, LM234, LM334

FEATURES

- **Operates From 1V to 40V**
- **0.02%/V Current Regulation**
- **Programmable From 1μA to 10mA**
- **True 2-Terminal Operation**
- **Available as Fully Specified Temperature Sensor**
- **±3% Initial Accuracy**

DESCRIPTION

The LM134/LM234/LM334 are 3-terminal adjustable current sources featuring 10,000:1 range in operating current, excellent current regulation and a wide dynamic voltage range of 1V to 40V. Current is established with one external resistor and no other parts are required. Initial current accuracy is ±3%. The LM134/LM234/LM334 are true floating current sources with no separate power supply connections. In addition, reverse applied voltages of up to 20V will draw only a few dozen microamperes of current, allowing the devices to act as both a rectifier and current source in AC applications.

The sense voltage used to establish operating current in the LM134 is 64mV at 25°C and is directly proportional to absolute temperature (°K). The simplest one external resistor connection, then, generates a current with ≈+0.33%/°C temperature dependence. Zero drift operation can be obtained by adding one extra resistor and a diode.

Applications for the current sources include bias networks, surge protection, low power reference, ramp generation, LED driver, and temperature sensing. The LM234-3 and LM234-6 are specified as true temperature sensors with ensured initial accuracy of ±3°C and ±6°C, respectively. These devices are ideal in remote sense applications because series resistance in long wire runs does not affect accuracy. In addition, only 2 wires are required.

The LM134 is specified over a temperature range of −55°C to +125°C, the LM234 from −25°C to +100°C and the LM334 from 0°C to +70°C. These devices are available in TO hermetic, TO-92 and SOIC-8 plastic packages.

Connection Diagrams

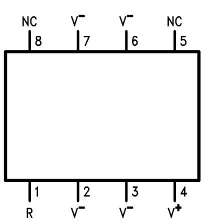


Figure 1. SOIC-8 Surface Mount Package (LM334M; LM334M/NOPB; LM334MX; LM334MX/NOPB) See Package Number D

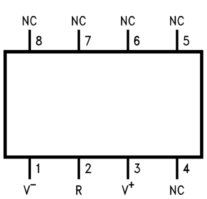


Figure 2. SOIC-8 Alternative Pinout Surface Mount Package (LM334SM; LM334SM/NOPB; LM334SMX; LM334SMX/NOPB) See Package Number D

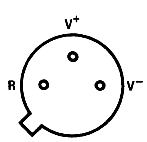


Figure 3. TO Metal Can Package (Bottom View) See Package Number NDV

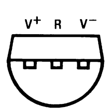


Figure 4. TO-92 Plastic Package (Bottom View) See Package Number LP

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

V^+ to V^- Forward Voltage		LM134/LM234/LM334	40V
		LM234-3/LM234-6	30V
V^+ to V^- Reverse Voltage			20V
R Pin to V^- Voltage			5V
Set Current			10 mA
Power Dissipation			400 mW
ESD Susceptibility(3)			2000V
Operating Temperature Range(4)		LM134	−55°C to +125°C
		LM234/LM234-3/LM234-6	−25°C to +100°C
		LM334	0°C to +70°C
Soldering Information	TO-92 Package (10 sec.)		260°C
	TO Package (10 sec.)		300°C
	SOIC Package	Vapor Phase (60 sec.)	215°C
		Infrared (15 sec.)	220°C

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human body model, 100pF discharged through a 1.5kΩ resistor.
(4) For elevated temperature operation, T_J max is:

LM134	150°C
LM234	125°C
LM334	100°C

See Thermal Characteristics.

Thermal Characteristics

over operating free-air temperature range (unless otherwise noted)

Thermal Resistance	TO-92	TO	SOIC-8
θ_{ja} (Junction to Ambient)	180°C/W (0.4″ leads)	440°C/W	165°C/W
	160°C/W (0.125″ leads)		
θ_{jc} (Junction to Case)	N/A	32°C/W	80°C/W

Electrical Characteristics(1)

Parameter	Conditions		LM134/LM234			LM334			Units
			Min	Typ	Max	Min	Typ	Max	
Set Current Error, V^+=2.5V(2)	10µA ≤ I_{SET} ≤ 1mA				3			6	%
	1mA < I_{SET} ≤ 5mA				5			8	%
	2µA ≤ I_{SET} < 10µA				8			12	%
Ratio of Set Current to Bias Current	100µA ≤ I_{SET} ≤ 1mA		14	18	23	14	18	26	
	1mA ≤ I_{SET} ≤ 5mA			14			14		
	2 µA≤I_{SET}≤100 µA			18	23		18	26	
Minimum Operating Voltage	2µA ≤ I_{SET} ≤ 100µA			0.8			0.8		V
	100µA < I_{SET} ≤ 1mA			0.9			0.9		V
	1mA < I_{SET} ≤ 5mA			1.0			1.0		V
Average Change in Set Current with Input Voltage	2µA ≤ I_{SET} ≤ 1mA	1.5 ≤ V^+ ≤ 5V		0.02	0.05		0.02	0.1	%/V
		5V ≤ V^+ ≤ 40V		0.01	0.03		0.01	0.05	%/V
	1mA < I_{SET} ≤ 5mA	1.5V ≤ V ≤ 5V		0.03			0.03		%/V
		5V ≤ V ≤ 40V		0.02			0.02		%/V
Temperature Dependence of Set Current(3)	25µA ≤ I_{SET} ≤ 1mA		0.96T	T	1.04T	0.96T	T	1.04T	
Effective Shunt Capacitance				15			15		pF

(1) Unless otherwise specified, tests are performed at T_j = 25°C with pulse testing so that junction temperature does not change during test
(2) Set current is the current flowing into the V^+ pin. For the Basic 2-Terminal Current Source circuit shown in Figure 13. I_{SET} is determined by the following formula: I_{SET} = 67.7 mV/R_{SET} (@ 25°C). Set current error is expressed as a percent deviation from this amount. I_{SET} increases at 0.336%/°C @ T_j = 25°C (227 µV/°C).
(3) I_{SET} is directly proportional to absolute temperature (°K). I_{SET} at any temperature can be calculated from: $I_{SET} = I_o (T/T_o)$ where I_o is I_{SET} measured at T_o (°K).

Electrical Characteristics(1)

Parameter	Conditions		LM234-3			LM234-6			Units
			Min	Typ	Max	Min	Typ	Max	
Set Current Error, V^+=2.5V (2)	100µA ≤ I_{SET} ≤ 1mA				±1			±2	%
	T_J = 25°								
Equivalent Temperature Error					±3			±6	°C
Ratio of Set Current to Bias Current	100µA ≤ I_{SET} ≤ 1mA		14	18	26	14	18	26	
Minimum Operating Voltage	100µA I_{SET} ≤ 1mA			0.9			0.9		V
Average Change in Set Current with Input Voltage	100µA ≤ I_{SET} ≤ 1mA	1.5 ≤ V^+ ≤ 5V		0.02	0.05		0.02	0.01	%/V
		5V ≤ V^+ ≤ 30V		0.01	0.03		0.01	0.05	%/V
Temperature Dependence of Set Current(3)	100µA ≤ I_{SET} ≤ 1mA		0.98T	T	1.02T	0.97T	T	1.03T	
Equivalent Slope Error					±2			±3	%
Effective Shunt Capacitance				15			15		pF

(1) Unless otherwise specified, tests are performed at T_j = 25°C with pulse testing so that junction temperature does not change during test
(2) Set current is the current flowing into the V^+ pin. For the Basic 2-Terminal Current Source circuit shown in Figure 13. I_{SET} is determined by the following formula: I_{SET} = 67.7 mV/R_{SET} (@ 25°C). Set current error is expressed as a percent deviation from this amount. I_{SET} increases at 0.336%/°C @ T_j = 25°C (227 µV/°C).
(3) I_{SET} is directly proportional to absolute temperature (°K). I_{SET} at any temperature can be calculated from: $I_{SET} = I_o (T/T_o)$ where I_o is I_{SET} measured at T_o (°K).

Typical Performance Characteristics

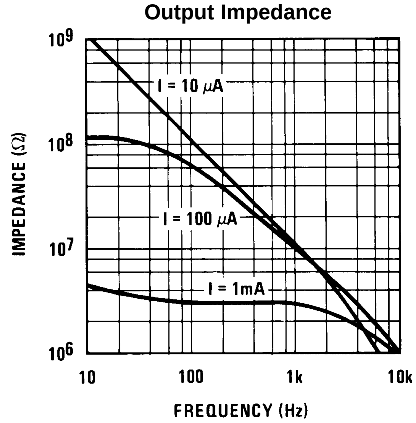


Figure 5.

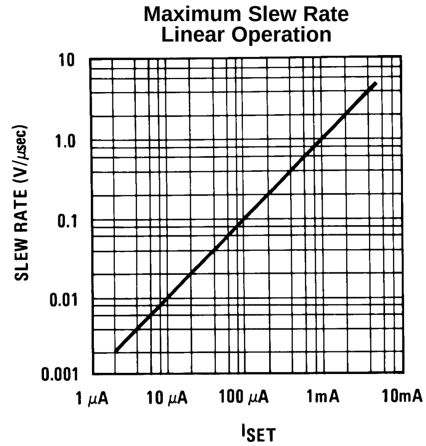


Figure 6.

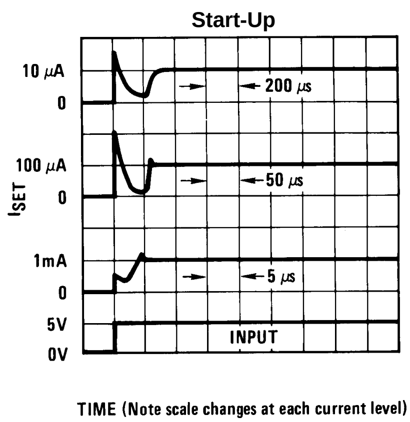


Figure 7.

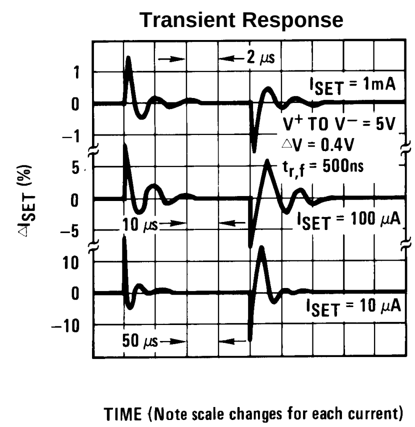


Figure 8.

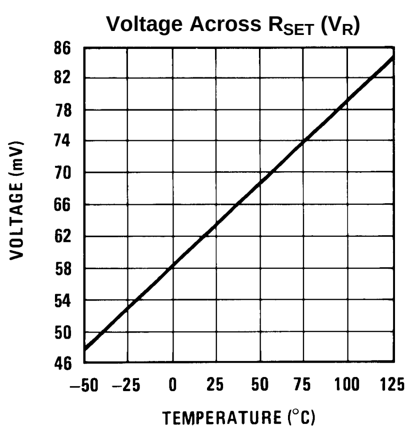


Figure 9.

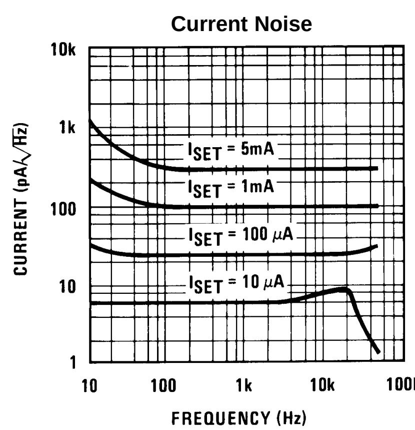


Figure 10.

Typical Performance Characteristics (continued)

Turn-On Voltage

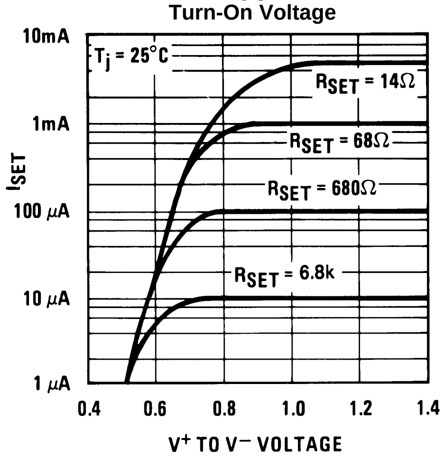


Figure 11.

Ratio of I_{SET} to I_{BIAS}

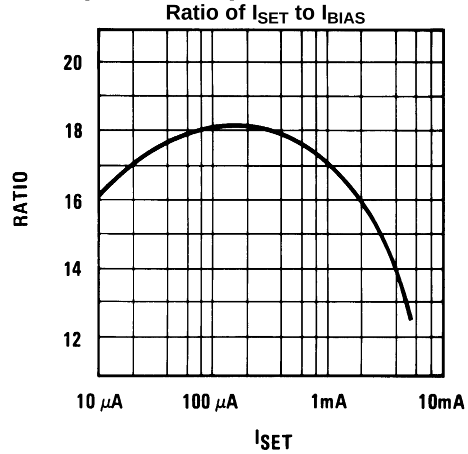


Figure 12.

APPLICATION HINTS

The LM134 has been designed for ease of application, but a general discussion of design features is presented here to familiarize the designer with device characteristics which may not be immediately obvious. These include the effects of slewing, power dissipation, capacitance, noise, and contact resistance.

Calculating R_{SET}

The total current through the LM134 (I_{SET}) is the sum of the current going through the SET resistor (I_R) and the LM134's bias current (I_{BIAS}), as shown in Figure 13.

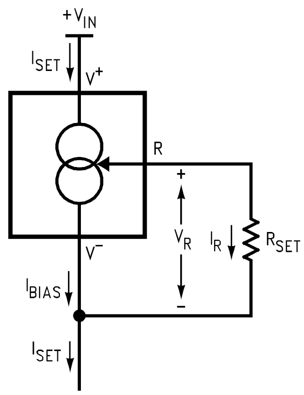


Figure 13. Basic Current Source

A graph showing the ratio of these two currents is supplied under **Ratio of I_{SET} to I_{BIAS}** in Typical Performance Characteristics. The current flowing through R_{SET} is determined by V_R, which is approximately 214μV/°K (64 mV/298°K ~ 214μV/°K).

$$I_{SET} = I_R + I_{BIAS} = \frac{V_R}{R_{SET}} + I_{BIAS} \quad (1)$$

Since (for a given set current) I_{BIAS} is simply a percentage of I_{SET}, the equation can be rewritten

$$I_{SET} = \left(\frac{V_R}{R_{SET}}\right)\left(\frac{n}{n-1}\right)$$

where

- n is the ratio of I_{SET} to I_{BIAS} as specified in Electrical Characteristics and shown in the graph (2)

Since n is typically 18 for 2μA ≤ I_{SET} ≤ 1mA, the equation can be further simplified to

$$I_{SET} = \left(\frac{V_R}{R_{SET}}\right)(1.059) = \frac{227\ \mu V/°K}{R_{SET}} \quad (3)$$

for most set currents.

Slew Rate

At slew rates above a given threshold (see curve), the LM134 may exhibit non-linear current shifts. The slewing rate at which this occurs is directly proportional to I_{SET}. At I_{SET} = 10μA, maximum dV/dt is 0.01V/μs; at I_{SET} = 1mA, the limit is 1V/μs. Slew rates above the limit do not harm the LM134, or cause large currents to flow.

Thermal Effects

Internal heating can have a significant effect on current regulation for I_{SET} greater than 100μA. For example, each 1V increase across the LM134 at I_{SET} = 1 mA will increase junction temperature by ≈0.4°C in still air. Output current (I_{SET}) has a temperature coefficient of ≈0.33%/°C, so the change in current due to temperature rise will be (0.4) (0.33) = 0.132%. This is a 10:1 degradation in regulation compared to true electrical effects. Thermal effects, therefore, must be taken into account when DC regulation is critical and I_{SET} exceeds 100μA. Heat sinking of the TO package or the TO-92 leads can reduce this effect by more than 3:1.

Shunt Capacitance

In certain applications, the 15 pF shunt capacitance of the LM134 may have to be reduced, either because of loading problems or because it limits the AC output impedance of the current source. This can be easily accomplished by buffering the LM134 with an FET as shown in the applications. This can reduce capacitance to less than 3 pF and improve regulation by at least an order of magnitude. DC characteristics (with the exception of minimum input voltage), are not affected.

Noise

Current noise generated by the LM134 is approximately 4 times the shot noise of a transistor. If the LM134 is used as an active load for a transistor amplifier, input referred noise will be increased by about 12dB. In many cases, this is acceptable and a single stage amplifier can be built with a voltage gain exceeding 2000.

Lead Resistance

The sense voltage which determines operating current of the LM134 is less than 100mV. At this level, thermocouple or lead resistance effects should be minimized by locating the current setting resistor physically close to the device. Sockets should be avoided if possible. It takes only 0.7Ω contact resistance to reduce output current by 1% at the 1 mA level.

Sensing Temperature

The LM134 makes an ideal remote temperature sensor because its current mode operation does not lose accuracy over long wire runs. Output current is directly proportional to absolute temperature in degrees Kelvin, according to the following formula:

$$I_{SET} = \frac{(227\ \mu V/°K)\ (T)}{R_{SET}} \tag{4}$$

Calibration of the LM134 is greatly simplified because of the fact that most of the initial inaccuracy is due to a gain term (slope error) and not an offset. This means that a calibration consisting of a gain adjustment only will trim both slope and zero at the same time. In addition, gain adjustment is a one point trim because the output of the LM134 extrapolates to zero at 0°K, independent of R_{SET} or any initial inaccuracy.

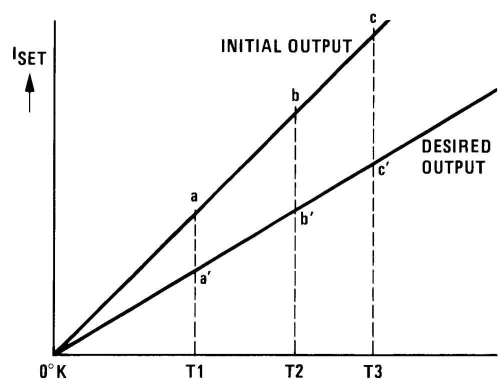


Figure 14. Gain Adjustment

This property of the LM134 is illustrated in the accompanying graph. Line abc is the sensor current before trimming. Line a′b′c′ is the desired output. A gain trim done at T2 will move the output from b to b′ and will simultaneously correct the slope so that the output at T1 and T3 will be correct. This gain trim can be done on R_{SET} or on the load resistor used to terminate the LM134. Slope error after trim will normally be less than ±1%. To maintain this accuracy, however, a low temperature coefficient resistor must be used for R_{SET}.

A 33 ppm/°C drift of R_{SET} will give a 1% slope error because the resistor will normally see about the same temperature variations as the LM134. Separating R_{SET} from the LM134 requires 3 wires and has lead resistance problems, so is not normally recommended. Metal film resistors with less than 20 ppm/°C drift are readily available. Wire wound resistors may also be used where best stability is required.

Application as a Zero Temperature Coefficent Current Source

Adding a diode and a resistor to the standard LM134 configuration can cancel the temperature-dependent characteristic of the LM134. The circuit shown in Figure 15 balances the positive tempco of the LM134 (about +0.23 mV/°C) with the negative tempco of a forward-biased silicon diode (about −2.5 mV/°C).

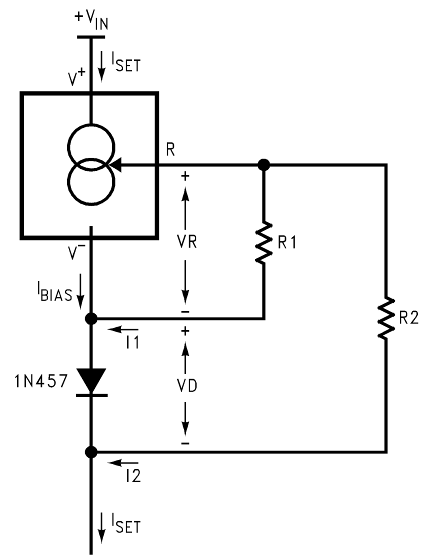


Figure 15. Zero Tempco Current Source

The set current (I_{SET}) is the sum of I_1 and I_2, each contributing approximately 50% of the set current, and I_{BIAS}. I_{BIAS} is usually included in the I_1 term by increasing the V_R value used for calculations by 5.9%. (See **CALCULATING R_{SET}**.)

$$I_{SET} = I_1 + I_2 + I_{BIAS}, \text{ where}$$

$$I_1 = \frac{V_R}{R_1} \quad \text{and} \quad I_2 = \frac{V_R + V_D}{R_2} \tag{5}$$

The first step is to minimize the tempco of the circuit, using the following equations. An example is given using a value of +227μV/°C as the tempco of the LM134 (which includes the I_{BIAS} component), and −2.5 mV/°C as the tempco of the diode (for best results, this value should be directly measured or obtained from the manufacturer of the diode).

$$\begin{aligned} I_{SET} &= I_1 + I_2 \\ \frac{dI_{SET}}{dT} &= \frac{dI_1}{dT} + \frac{dI_2}{dT} \\ &\approx \frac{227\ \mu V/°C}{R_1} + \frac{227\ \mu V/°C - 2.5\ mV/°C}{R_2} \\ &= 0 \text{ (solve for tempco } = 0) \end{aligned} \tag{6}$$

$$\frac{R_2}{R_1} \approx \frac{2.5\ mV/°C - 227\ \mu V/°C}{227\ \mu V/°C} \approx 10.0 \tag{7}$$

With the R_1 to R_2 ratio determined, values for R_1 and R_2 should be determined to give the desired set current. The formula for calculating the set current at T = 25°C is shown below, followed by an example that assumes the forward voltage drop across the diode (V_D) is 0.6V, the voltage across R_1 is 67.7mV (64 mV + 5.9% to account for I_{BIAS}), and R_2/R_1 = 10 (from the previous calculations).

$$I_{SET} = I_1 + I_2 + I_{BIAS}$$
$$= \frac{V_R}{R_1} + \frac{V_R + V_D}{R_2}$$
$$\approx \frac{67.7\text{ mV}}{R_1} + \frac{67.7\text{ mV} + 0.6\text{V}}{10.0\, R_1}$$
$$I_{SET} \approx \frac{0.134\text{V}}{R_1} \quad (8)$$

This circuit will eliminate most of the LM134's temperature coefficient, and it does a good job even if the estimates of the diode's characteristics are not accurate (as the following example will show). For lowest tempco with a specific diode at the desired I_{SET}, however, the circuit should be built and tested over temperature. If the measured tempco of I_{SET} is positive, R_2 should be reduced. If the resulting tempco is negative, R_2 should be increased. The recommended diode for use in this circuit is the 1N457 because its tempco is centered at 11 times the tempco of the LM134, allowing $R_2 = 10\ R_1$. You can also use this circuit to create a current source with non-zero tempcos by setting the tempco component of the tempco equation to the desired value instead of 0.

EXAMPLE: A 1mA, Zero-Tempco Current Source

First, solve for R_1 and R_2:

$$I_{SET} \approx 1\text{ mA} = \frac{0.134\text{V}}{R_1}$$
$$R_2 = 134\Omega = 10\, R_1$$
$$R_2 = 1340\Omega \quad (9)$$

The values of R_1 and R_2 can be changed to standard 1% resistor values ($R_1 = 133\Omega$ and $R_2 = 1.33\text{k}\Omega$) with less than a 0.75% error.

If the forward voltage drop of the diode was 0.65V instead of the estimate of 0.6V (an error of 8%), the actual set current will be

$$I_{SET} = \frac{67.7\text{ mV}}{R_1} + \frac{67.7\text{ mV} + 0.65\text{V}}{R_2}$$
$$= \frac{67.7\text{ mV}}{133} + \frac{67.7\text{ mV} + 0.65\text{V}}{1330}$$
$$= 1.049\text{ mA} \quad (10)$$

an error of less than 5%.

If the estimate for the tempco of the diode's forward voltage drop was off, the tempco cancellation is still reasonably effective. Assume the tempco of the diode is 2.6mV/°C instead of 2.5mV/°C (an error of 4%). The tempco of the circuit is now:

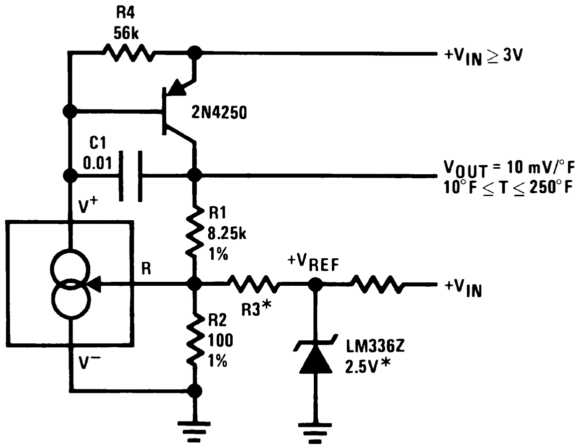
$$\frac{dI_{SET}}{dT} = \frac{dI_1}{dT} + \frac{dI_2}{dT}$$
$$= \frac{227\ \mu\text{V/°C}}{133\Omega} + \frac{227\ \mu\text{V/°C} - 2.6\text{ mV/°C}}{1330\Omega}$$
$$= -77\text{ nA/°C} \quad (11)$$

A 1mA LM134 current source with no temperature compensation would have a set resistor of 68Ω and a resulting tempco of

$$\frac{227\ \mu\text{V/°C}}{68\Omega} = 3.3\ \mu\text{A/°C} \quad (12)$$

So even if the diode's tempco varies as much as ±4% from its estimated value, the circuit still eliminates 98% of the LM134's inherent tempco.

Typical Applications



*Select R3 = V_{REF}/583µA. V_{REF} may be any stable positive voltage ≥ 2V
Trim R3 to calibrate

Figure 16. Ground Referred Fahrenheit Thermometer

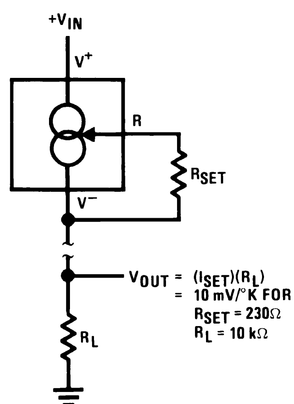
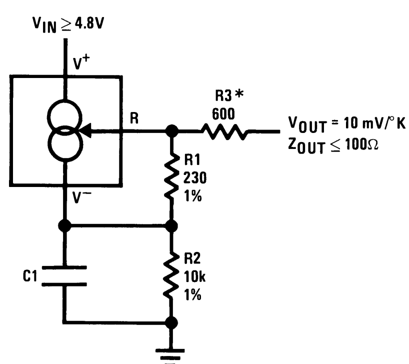


Figure 17. Terminating Remote Sensor for Voltage Output



*Output impedance of the LM134 at the "R" pin is approximately

$$\frac{-R_2}{16}$$

where R_2 is the equivalent external resistance connected from the V^- pin to ground. This negative resistance can be reduced by a factor of 5 or more by inserting an equivalent resistor $R_3 = (R_2/16)$ in series with the output.

Figure 18. Low Output Impedance Thermometer

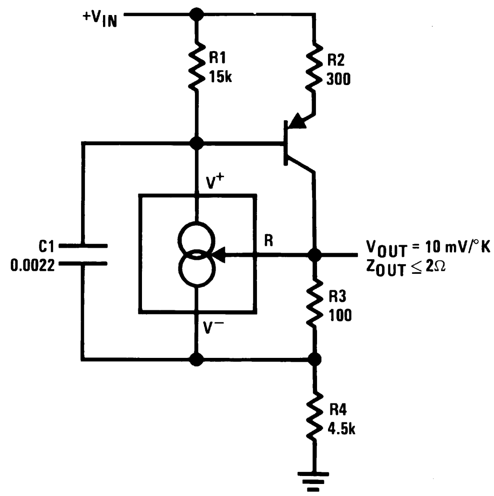
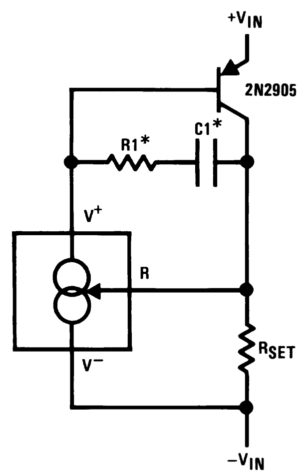


Figure 19. Low Output Impedance Thermometer



*Select R1 and C1 for optimum stability

Figure 20. Higher Output Current

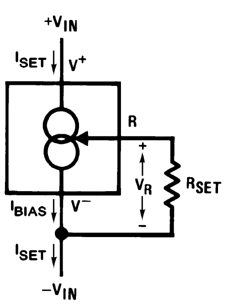


Figure 21. Basic 2-Terminal Current Source

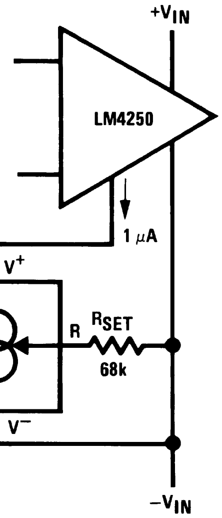


Figure 22. Micropower Bias

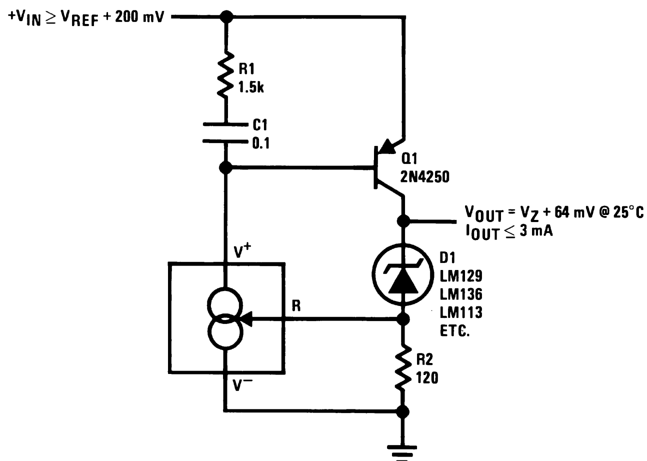


Figure 23. Low Input Voltage Reference Driver

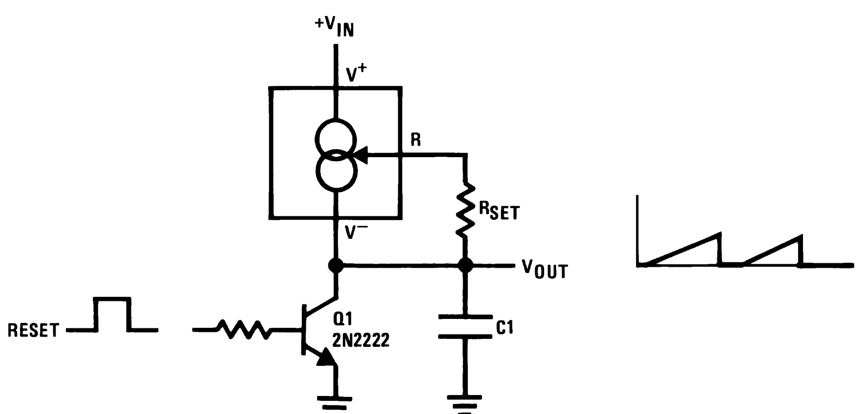
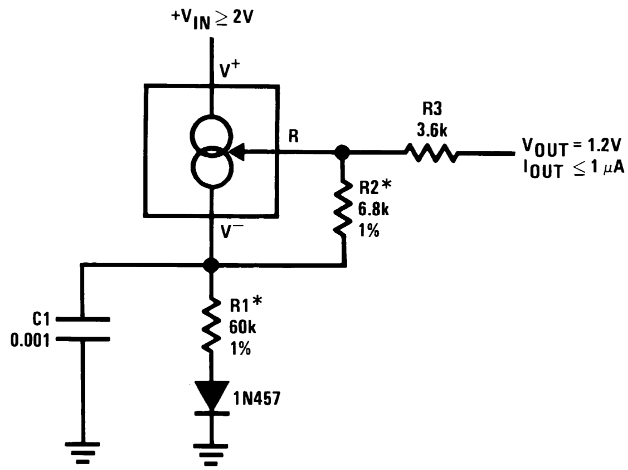
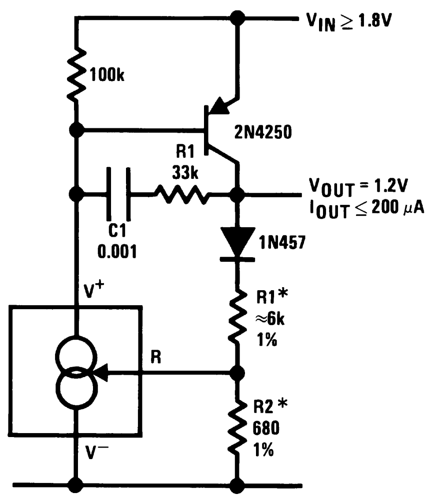


Figure 24. Ramp Generator



*Select ratio of R1 to R2 to obtain zero temperature drift

Figure 25. 1.2V Reference Operates on 10 µA and 2V



*Select ratio of R1 to R2 for zero temperature drift

Figure 26. 1.2V Regulator with 1.8V Minimum Input

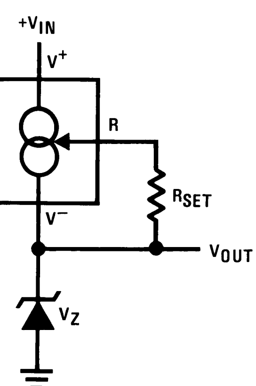
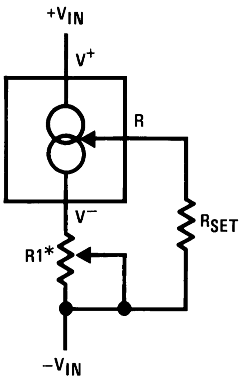


Figure 27. Zener Biasing



*For ±10% adjustment, select R_{SET} 10% high, and make R1 ≈ 3 R_{SET}

Figure 28. Alternate Trimming Technique

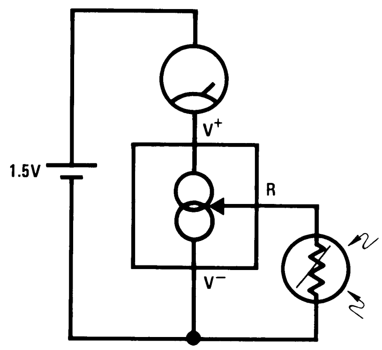
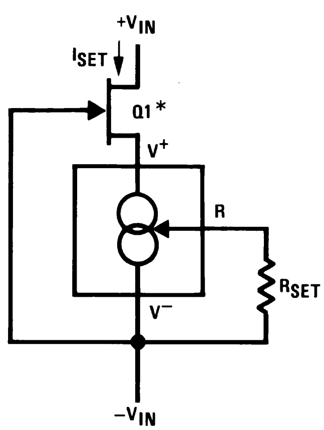


Figure 29. Buffer for Photoconductive Cell



*Select Q1 or Q2 to ensure at least 1V across the LM134. V_p (1 − I_{SET}/I_{DSS}) ≥ 1.2V.

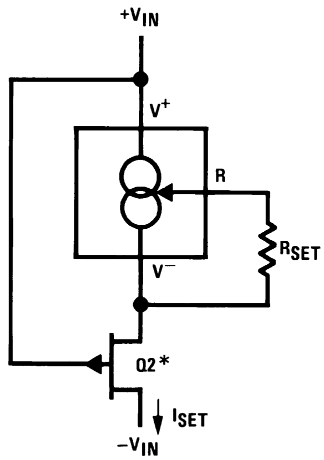
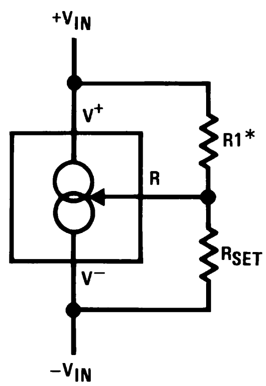
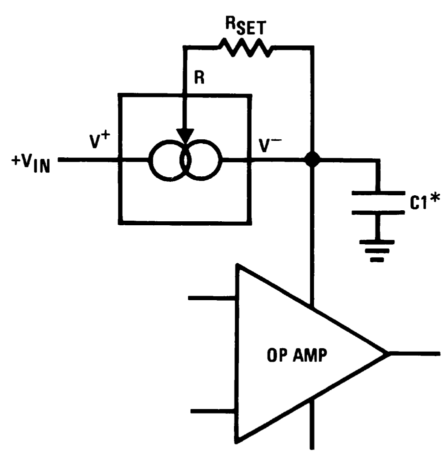


Figure 30. FET Cascoding for Low Capacitance and/or Ultra High Output Impedance



*$Z_{OUT} \approx -16 \bullet R1$ (R1/V_{IN} must not exceed I_{SET})

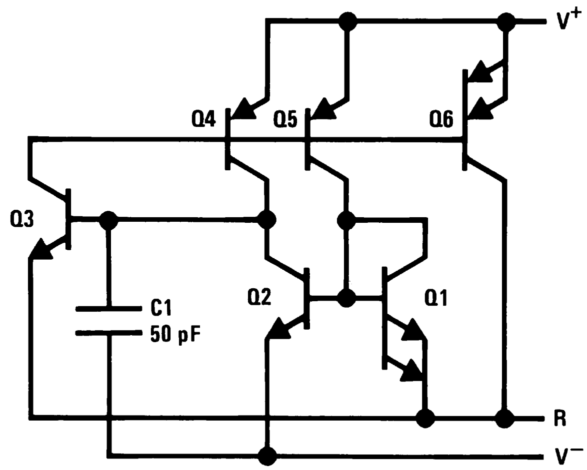
Figure 31. Generating Negative Output Impedance



*Use minimum value required to ensure stability of protected device. This minimizes inrush current to a direct short.

Figure 32. In-Line Current Limiter

Schematic Diagram



REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM134H	ACTIVE	TO	NDV	3	1000	TBD	Call TI	Call TI	-55 to 125	(LM134H ~ LM134H)	Samples
LM134H/NOPB	ACTIVE	TO	NDV	3	1000	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-55 to 125	(LM134H ~ LM134H)	Samples
LM234Z-3/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-25 to 100	LM234 Z-3	Samples
LM234Z-6/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-25 to 100	LM234 Z-6	Samples
LM334M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	LM334 M	
LM334M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM334 M	Samples
LM334MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM334 M	Samples
LM334SM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	LM334 SM	
LM334SM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM334 SM	Samples
LM334SMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	LM334 SM	
LM334SMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM334 SM	Samples
LM334Z/LFT1	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type		LM334 Z	Samples
LM334Z/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	0 to 70	LM334 Z	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

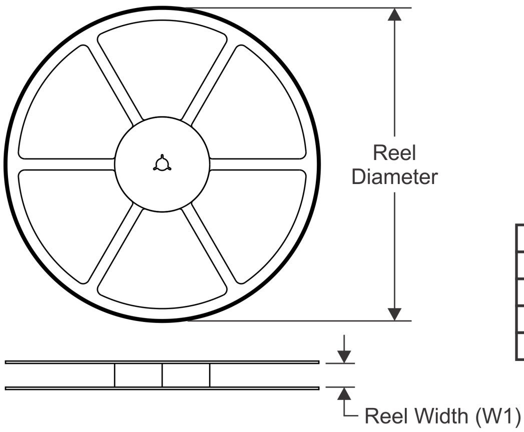
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

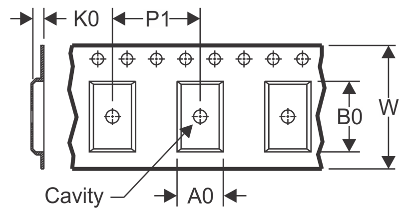
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

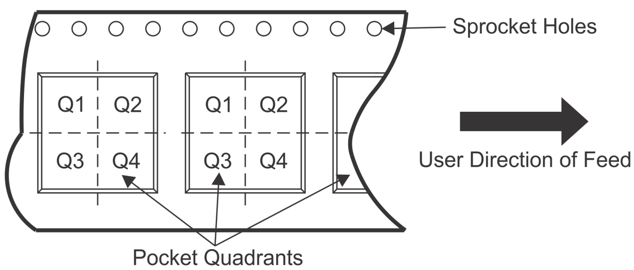


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

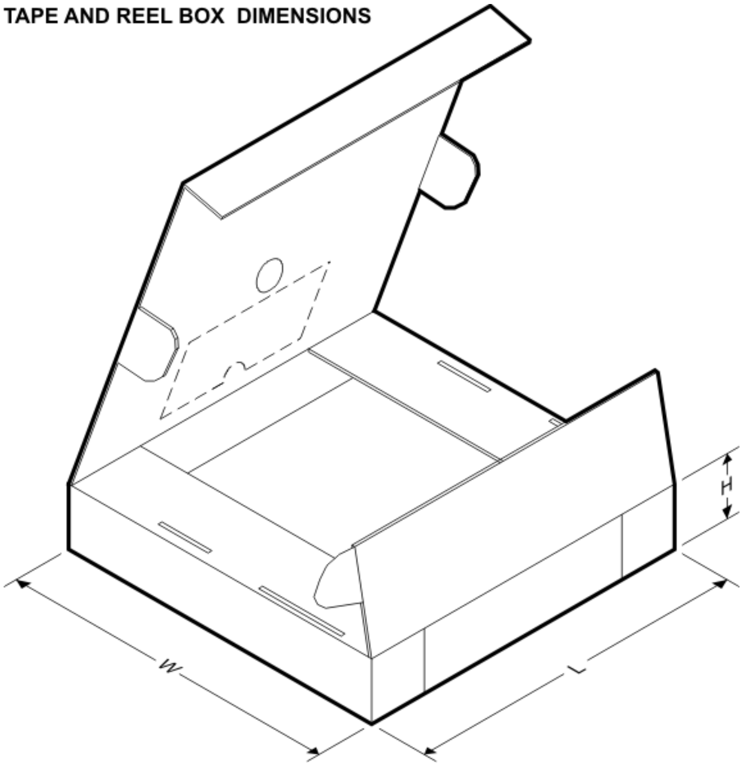
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM334MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM334SMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM334SMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

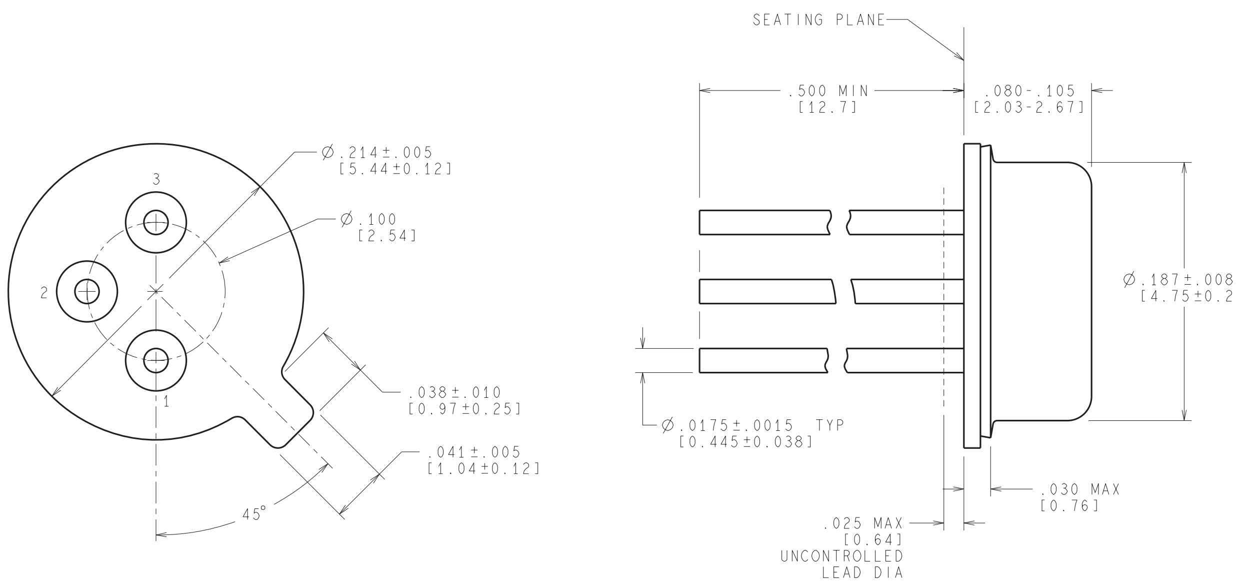
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM334MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM334SMX	SOIC	D	8	2500	367.0	367.0	35.0
LM334SMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

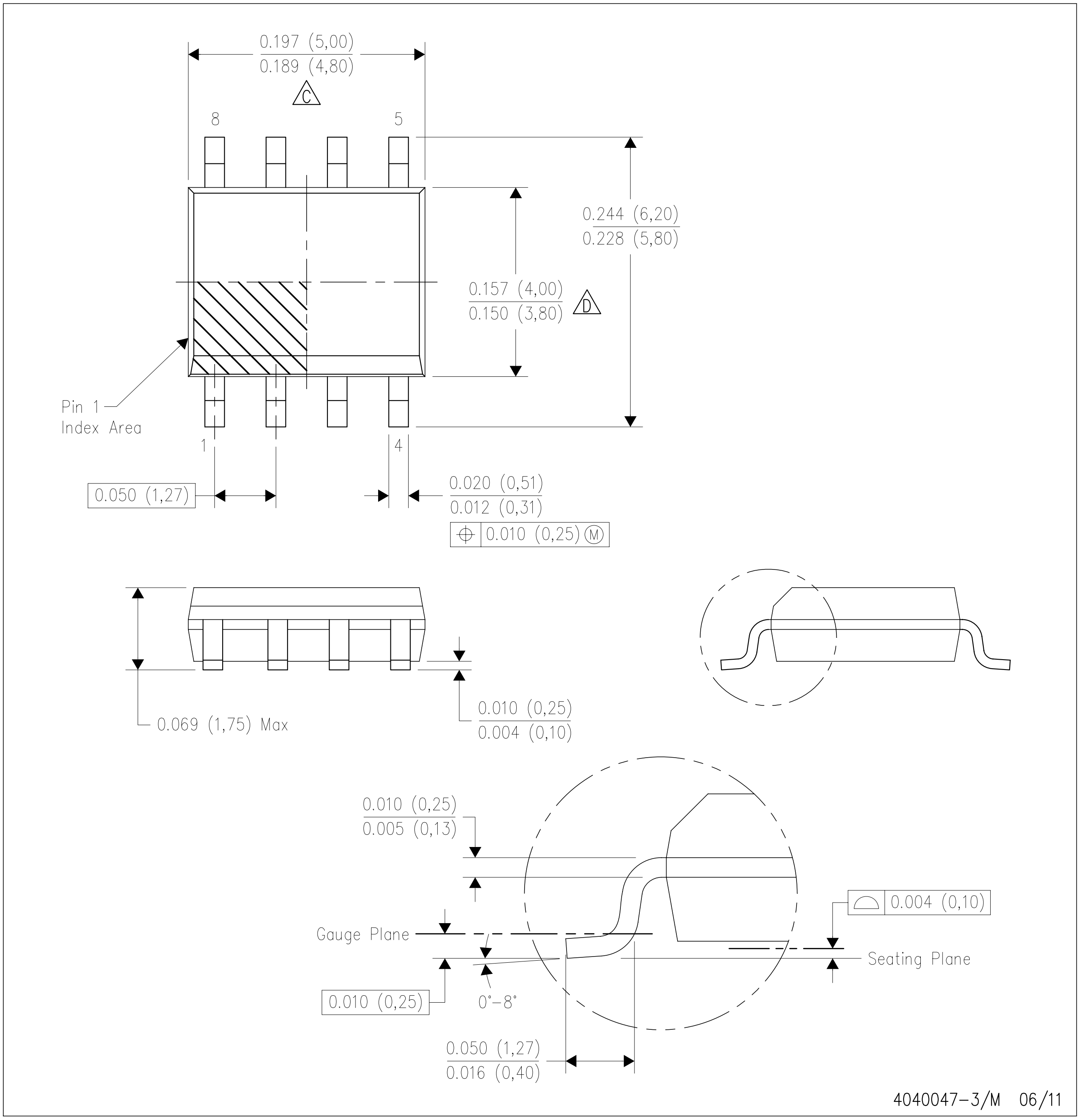
NDV0003H



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE IN MILLIMETERS

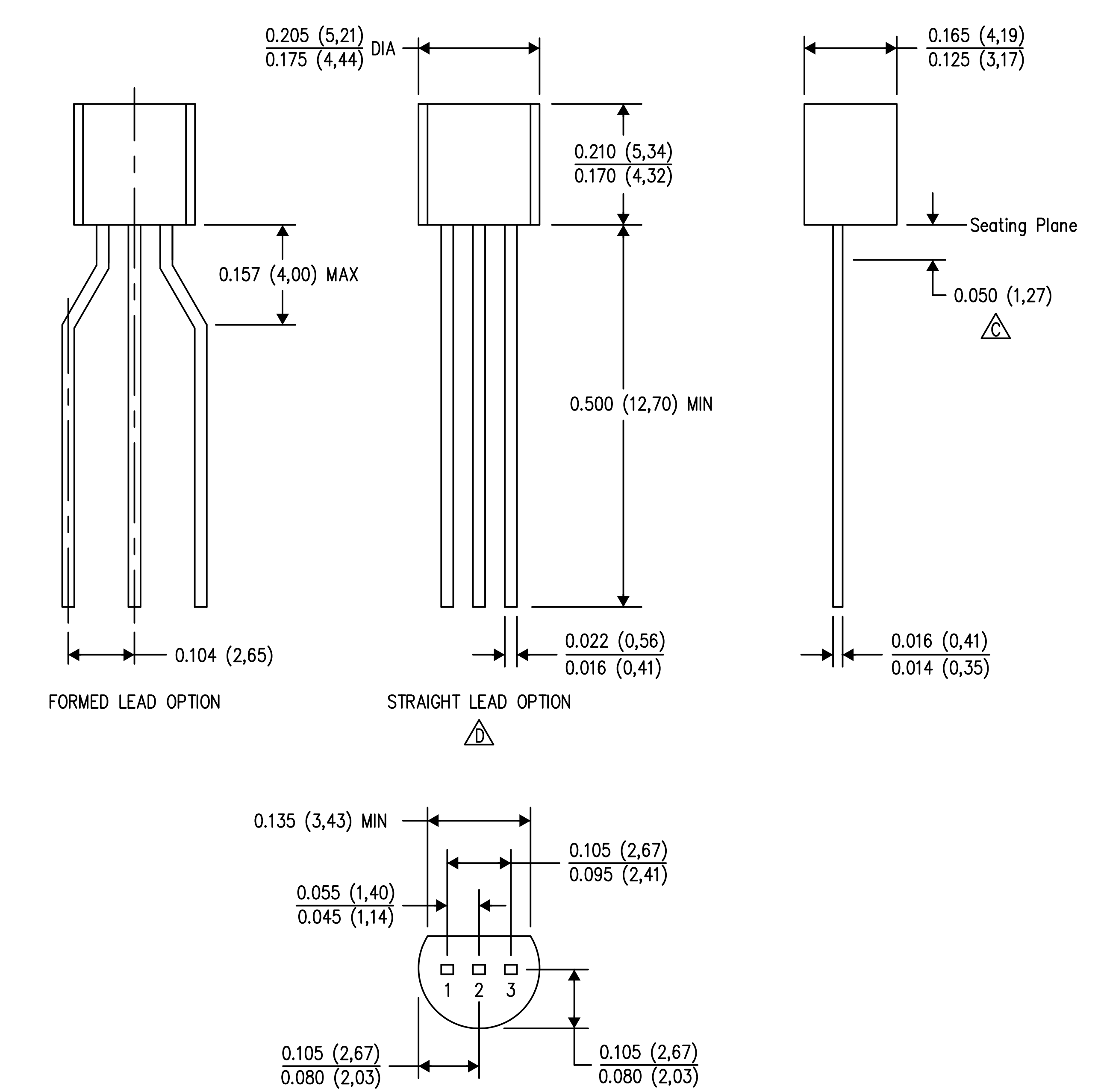
H03H (Rev F)

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

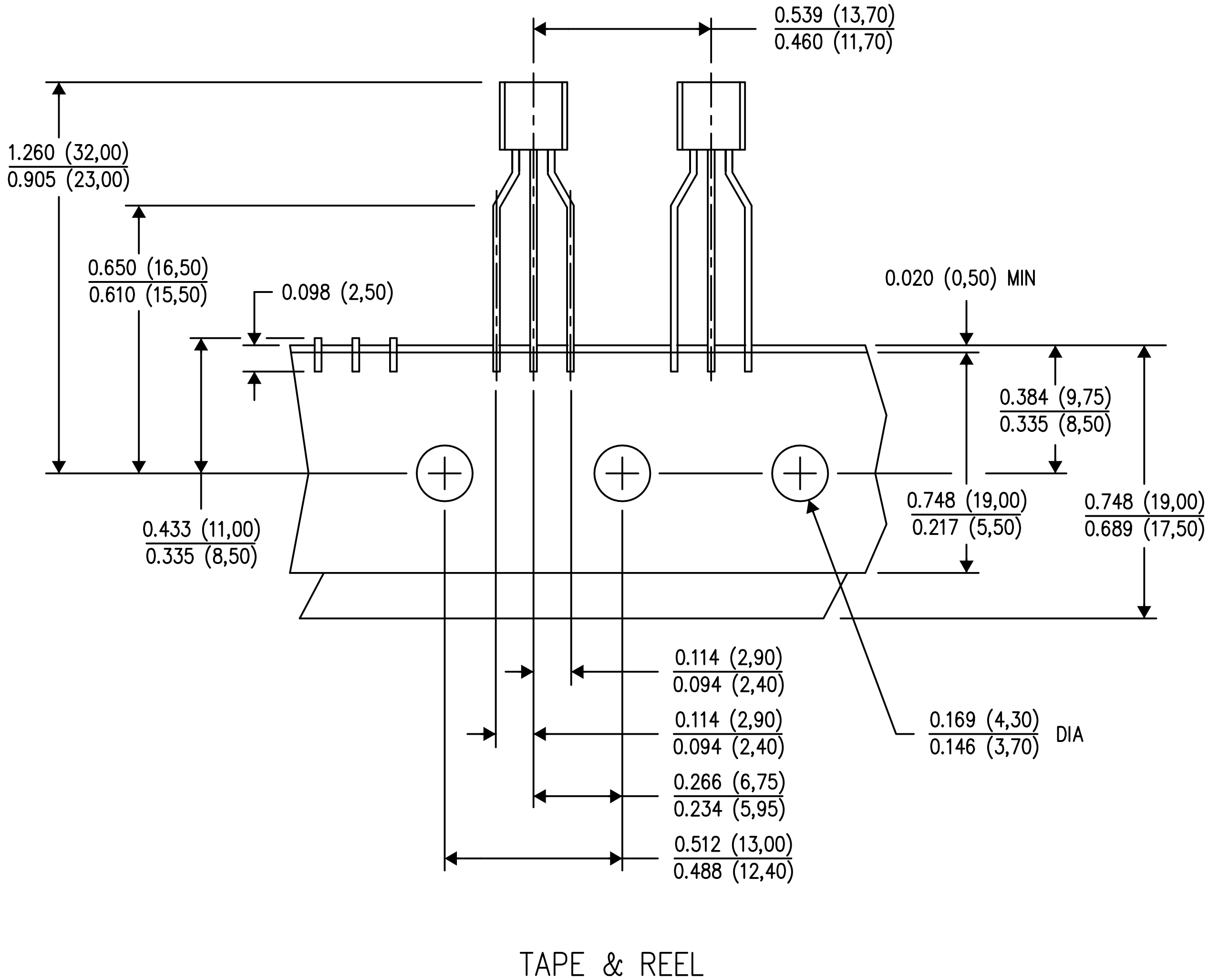
LP (O-PBCY-W3) PLASTIC CYLINDRICAL PACKAGE



4040001-2/E 08/13

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. Falls within JEDEC TO-226 Variation AA (TO-226 replaces TO-92).
- E. Shipping Method:
  Straight lead option available in bulk pack only.
  Formed lead option available in tape & reel or ammo pack.
  Specific products can be offered in limited combinations of shipping mediums and lead options.
  Consult product folder for more information on available options.

LP (O-PBCY-W3) PLASTIC CYLINDRICAL PACKAGE



4040001-3/E 08/13

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Tape and Reel information for the Formed Lead Option package.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265